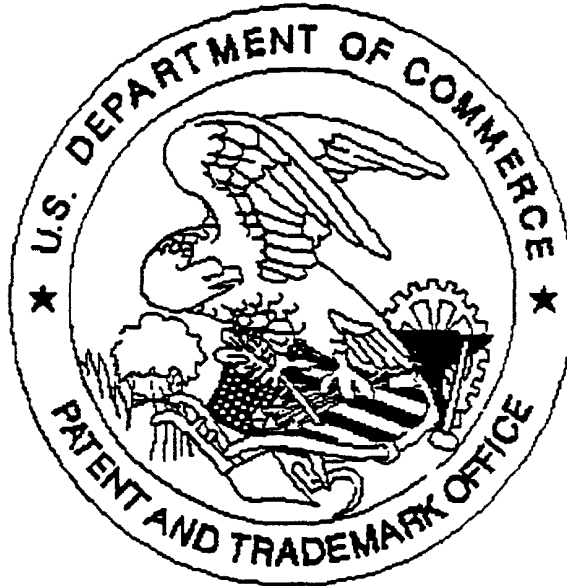


REFERENCE NUMERALS

	first TAP 12, called Master TAP	[5]
	eTAP1 14	[5]
5	eTAP2 16	[5]
	processor cores 18 and 20	[7]
	first group 22 of TAPs	[7]
	second group 24	[7]
	shift register 30	[8]
10	update register 32	[9]
	multiplexer 34	[9]
	shift register 36	[9]
	an associated update register 38	[9]
	multiplexer 40	[10]
15	TDO multiplexer 42	[11]
	TMS gating circuit 50	[11]
	RESET gating circuit 52	[12]
	Master TAP 100	[12]
	embedded TAPS 102, 104 and 106	[12]
20	three TAP groups 110, 112 and 114	[12]
	instruction register 116	[13]
	instruction registers 118 and 120	[13]
	group TDI node 122	[13]
	group TDO node 124	[13]
25	instruction register 125 of the Master TAP	[13]
	TDI input 126	[13]
	TDI multiplexers 132 and 134 associated with embedded TAP groups 112 and 114, respectively	[14]
	a data register, such as shown by reference numeral 136 in FIG. 3	[16]
30	circuit 60	[17]
	Master TAP 62	[17]
	test data register 64	[17]
	embedded TAP 66	[17]
	multiplexer 70	[17]
35	a multiplexer 72	[17]

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